CLAIMS

What is claimed is:

1. A pulse width modulation controlling circuit for a power supply comprising:

a processor means for generating a time-length signal comprising a first and second portion;

a counting means for receiving said first portion of said time-length signal and counting in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal said counting means outputting said coarse adjusted signal;

a delay means operatively connected to said counting means for receiving said coarse adjusted signal; and

a selection means coupled to said delay means for receiving said second portion of said time-length signal and for selecting a predetermined discrete delay period in said delay means, for creating discrete time steps, whereby said power supply is capable of providing a plurality of repeatable output pulses.

2. The apparatus of claim 1, wherein said counting means is a digital counting means.

3. The apparatus of claim 2, wherein said digital counting means comprises a programmable logic device.

4. The apparatus of claim 3, wherein said counting means comprises an oscillator means operating at a predetermined frequency.

5. The apparatus of claim 4, wherein said oscillator means oscillates at approximately 125 MHz.

6. The apparatus of claim 1, wherein said delay means delays in increments of 0.25 nanoseconds.

7. The apparatus of claim 1, wherein said delay means is an analog delay means.

8. The apparatus of claim 1, wherein said delay means is a digital delay means.

9. The apparatus of claim 7, wherein said delay means comprises a plurality of inductors and capacitors connected in a series-parallel configuration.

10. The apparatus of claim 1, wherein said selection means is a digital selection means.

11. The apparatus of claim 9, wherein said selection means is a multiplexor.

12. The apparatus of claim 1, wherein said processor means operates at a first voltage, and said counting means, delay means, and selection means operates at a second voltage.

13. The apparatus of claim 12, wherein said apparatus further comprises a first and second transforming means, a power converter means, and a power conditioning means, wherein an output of said processing means

is coupled to said first transforming means for transforming said output of said processing means at said first voltage to said second voltage, and an output of said second selection means is coupled to said power converting means, said second transformer means, and said power conditioning means.

14. The apparatus of claim 1, wherein said counting means, said delay means and said selection means are disposed in said processing means.

15. A method for controlling a switchmode power supply comprising:

generating a time-length signal;

transmitting a first portion of said time-length signal to a counting means, and a second portion of said time-length signal to a selection means;

counting to a number based on said first portion of said time-length signal received by said counting means;

outputting a coarse adjusted signal from said counting means after counting to said predetermined number;

selecting a delay from a delay means based on said second portion of said time-length signal received by said selection means;

delaying said coarse adjusted signal a predetermined length of time based on said selected delay in said delay means; and

outputting an output signal after said predetermined delay.

16. A pulse width modulation controlling circuit for a power supply comprising:

a processor means for generating a time-length signal comprising a first and second portion;

a first selection means for receiving said first portion of said time-length signal, and for selecting one of a plurality of counting means, wherein said selected one of said plurality of counting means receives said first portion of said time-length signal and counts in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal, said selected one of said plurality of counting means outputting said coarse adjusted signal;

a delay means operatively connected to said counting means for receiving said coarse adjusted signal; and

a second selection means coupled to said delay means for receiving said second portion of said time-length signal and for selecting a predetermined discrete delay period in said delay means, for creating discrete time steps, whereby said power supply is capable of providing a plurality of repeatable output pulses.

17. The apparatus of claim 16, wherein each one of said plurality of counting means counts at a unique, predetermined rate.

18. The apparatus of claim 16, wherein said plurality of counting means are digital counting means.

19. The apparatus of claim 16, wherein said each one of said plurality of counting means comprises a programmable logic device.

20. The apparatus of claim 16, wherein said counting means comprises an oscillator means operating at a predetermined frequency.

21. The apparatus of claim 16, wherein said delay means is an analog delay means.

22. The apparatus of claim 16, wherein said delay means is a digital delay means.

23. The apparatus of claim 21, wherein said delay means comprises a plurality of inductor and capacitors connected in a series-parallel configuration.

24. The apparatus of claim 16, wherein said first selection means is a digital selection means.

25. The apparatus of claim 24, wherein said first selection means is a multiplexor.

26. The apparatus of claim 16, wherein said second selection means is a digital selection means.

27. The apparatus of claim 26, wherein said second selection means is a multiplexor.

28. The apparatus of claim 16, where in said processor means operates at a first voltage, and said first selection means, said plurality of counting means, delay means, and second selection means operates at a second voltage.

29. The apparatus of claim 28, wherein said apparatus further comprises a first and second transforming means, a power converter means, and a power conditioning means, wherein an output of said processing means is coupled to said first transforming means for transforming said output of

said processing means at said first voltage to said second voltage, and an output of said second selection means is coupled to said power converting means, said second transformer means, and said power conditioning means.

30. The apparatus of claim 16, wherein said counting means, said delay means and said selection means are disposed in said processing means.

31. A pulse width modulation controlling circuit for a power supply comprising:

a processor means for generating a time-length signal comprising a first portion and second portion;

a counting means for receiving said first portion of said time-length signal and counting in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal, said counting means outputting said coarse adjusted signal;

a delay selection means for receiving said second portion of said time-length signal;

a plurality of delay means operatively connected to said plurality of counting means for receiving said coarse adjusted signal; and

a plurality of second selector means, wherein said delay selection means selects one of said plurality of second selector means, and wherein a second selector means is coupled to each one of said plurality of delay means, said selected one of said plurality of second selector means for selecting a predetermined discrete delay period in one of said plurality of delay means,

for creating discrete time steps, whereby said power supply is capable of providing a plurality of repeatable output pulses.

32. The apparatus of claim 31, wherein said counting means is a digital counting means.

33. The apparatus of claim 32, wherein said digital counting means comprises a programmable logic device.

34. The apparatus of claim 33, wherein said counting means comprises an oscillator means operating at a predetermined frequency.

35. The apparatus of claim 34, wherein said oscillator means oscillates at approximately 125 MHz.

36. The apparatus of claim 31, wherein said delay means delays in increments of 0.25 nanoseconds.

37. The apparatus of claim 31, wherein said delay selection means is a digital delay selection means.

38. The apparatus of claim 37, wherein said delay selection means is a multiplexor.

39. The apparatus of claim 31, wherein said plurality of second selector means are digital selector means.

40. The apparatus of claim 39, wherein said plurality of second selector means are multiplexors

41. The apparatus of claim 31, wherein each one of said plurality of delay means delays said coarse adjusted signal in unique, predetermined increments.

42. The apparatus of claim 31, wherein each one of said plurality of delay means is an analog delay means.

43. The apparatus of claim 42, wherein each one of said plurality of delay means comprises a plurality of inductor and capacitors connected in a series-parallel configuration.

44. The apparatus of claim 31, wherein each one of said plurality of delay means is a digital delay means.

45. The apparatus of claim 31, wherein said processor means operates at a first voltage, and said counting means, delay selection means, plurality of delay means, plurality of second and said selector means, operates at a second voltage.

46. The apparatus of claim 45, wherein said apparatus further comprises a first and second transforming means, a power converter means, and a power conditioning means, wherein an output of said processing means is coupled to said first transforming means for transforming said output of said processing means at said first voltage to said second voltage, and an output of each one of said plurality of second selector means, said selection means is coupled to power converting means, said second transformer means, and said power conditioning means.

47. The apparatus of claim 31, wherein said counting means, said delay means and said selection means are disposed in said processing means.

48. A pulse width modulation controlling circuit for a power supply comprising:

a processor means for generating a time-length signal comprising a first and second portion;

a first selection means for receiving said first portion of said time-length signal, and for selecting one of a plurality of counting means, wherein said selected one of said plurality of counting means receives said first portion of said time-length signal and counts in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal, said selected one of said plurality of counting means outputting said coarse adjusted signal;

a delay selection means for receiving said second portion of said time-length signal;

a plurality of delay means operatively connected to said plurality of counting means for receiving said coarse adjusted signal; and

a plurality of second selector means, wherein said delay selection means selects one of said plurality of second selector means, and wherein a second selector means is coupled to each one of said plurality of delay means, said selected one of said plurality of second selector means for selecting a predetermined discrete delay period in one of said plurality of delay means, for creating discrete time steps, whereby said power supply is capable of providing a plurality of repeatable output pulses.

49. The apparatus of claim 48, wherein each one of said plurality of counting means counts at a unique, predetermined rate.

50. The apparatus of claim 48, wherein said plurality of counting means are digital counting means.

51. The apparatus of claim 48, wherein said first selection means is a digital selection means.

52. The apparatus of claim 48, wherein said first selection means is a multiplexor.

53. The apparatus of claim 48, wherein said delay selection means is a digital delay selection means.

54. The apparatus of claim 53, wherein said delay selection means is a multiplexor.

55. The apparatus of claim 48, wherein said plurality of second selector means are digital selector means.

56. The apparatus of claim 55, wherein said plurality of second selector means are multiplexors.

57. The apparatus of claim 48, wherein each one of said plurality of delay means delays said coarse adjusted signal in unique, predetermined increments.

58. The apparatus of claim 48, wherein each one of said plurality of delay means is an analog delay means.

59. The apparatus of claim 58, wherein each one of said plurality of delay means comprises a plurality of inductor and capacitors connected in a series-parallel configuration.

60. The apparatus of claim 48, wherein each one of said plurality of delay means is a digital delay means.

61. The apparatus of claim 48, wherein said processing means operates at a first voltage, and said first selection means, plurality of counting means, delay selection means, plurality of delay means and said plurality of second selector means operates at a second voltage.

62. The apparatus of claim 61, wherein said apparatus further comprises a first and second transforming means, a power converter means, and a power conditioning means, wherein an output of said processing means is coupled to said first transforming means for transforming said output of said processing means at said first voltage to said second voltage, and an output of each one of said plurality of second selector means is coupled to power converting means, said second transformer means, and said power conditioning means.

63. The apparatus of claim 48, wherein said counting means, said delay means and said selection means are disposed in said processing means.

64. A method for controlling a switchmode power supply in a plasma chamber comprising:

generating a time-length signal;

transmitting a first portion of said time-length signal to a counting means, and a second portion of said time-length signal to a selection means;

counting to a number based on said first portion of said time-length signal received by said counting means;

outputting a coarse adjusted signal from said counting means after counting to said predetermined number;

selecting a delay from a delay means based on said second portion of said time-length signal received by said selection means;

delaying said coarse adjusted signal a predetermined length of time based on said selected delay in said delay means; and

outputting an output signal to said power supply in said plasma chamber after said predetermined delay.

65. The apparatus of claim 64, wherein said counting means is a digital counting means.

66. The apparatus of claim 65, wherein said digital counting means comprises a programmable logic device.

67. The apparatus of claim 66, wherein said counting means comprises an oscillator means operating at a predetermined frequency.

68. The apparatus of claim 67, wherein said oscillator means oscillates at approximately 125 MHz.

69. The apparatus of claim 64, wherein said delay means delays in increments of 0.25 nanoseconds.

70. The apparatus of claim 64, wherein said delay means is an analog delay means.

71. The apparatus of claim 64, wherein said delay means is a digital delay means.

72. The apparatus of claim 70, wherein said delay means comprises a plurality of inductors and capacitors connected in a series-parallel configuration.

73. The apparatus of claim 64, wherein said selection means is a digital selection means.

74. The apparatus of claim 64, wherein said selection means is a multiplexor.

75. The apparatus of claim 64, wherein said processor means operates at a first voltage, and said counting means, delay means, and selection means operates at a second voltage.

76. The apparatus of claim 75, wherein said apparatus further comprises a first and second transforming means, a power converter means, and a power conditioning means, wherein an output of said processing means is coupled to said first transforming means for transforming said output of said processing means at said first voltage to said second voltage, and an output of said second selection means is coupled to said power converting means, said second transformer means, and said power conditioning means.

77. The apparatus of claim 64, wherein said counting means, said delay means and said selection means is disposed in said processing means.

78. The process of claim 64, wherein the step of generating a time-length signal further comprises generating said time-length signal in a processor means.

79. The process of claim 64, wherein said counting means is a digital counting means.